BARNABOSS PULI

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PROFESSIONAL SUMMARY

Master's in Computer Engineering graduate from California State University, Fullerton (CGPA: 3.95/4), with a strong foundation in machine learning, hardware validation, and system-level debugging. Experienced in FPGA security, embedded systems, and full-stack development, with hands-on expertise in hardware/software co-design and ML-driven validation methodologies. Adept at using machine learning for hardware security, performance optimization, and anomaly detection. Passionate about hardware validation, ML for reliability testing, and FPGA-based acceleration

TECHNICAL SKILLS

Programing Languages: Python, Java, C++, Embedded C, JavaScript, TypeScript, Go, Verilog HDL, GraphQL, Scala
Machine Learning: TensorFlow, PyTorch, Scikit-learn, ONNX, ML Model Optimization, Bayesian Optimization
System and Hardware Debugging: Power Analysis, Timing Optimization, RTL Debugging, Signal Integrity Analysis
Tools & Software: Synopsys, Cadence, MATLAB & Simulink, Docker, Git, NVIDIA Nsight, Jupyter Notebook
Hardware Testing & Verification: JTAG Debugging, FPGA Prototyping, Hardware Monte Carlo Simulations, HSPICE

RESEARCH EXPERIENCE

Research Assistant, California State University, Fullerton **Aug. 2023-Dec. 2024**

- Led a groundbreaking research project focused on FPGA security, emphasizing the application of advanced machine learning methodologies to detect hardware Trojans, showcasing proficiency in both hardware and software aspects.
- Implemented dynamic partial reconfiguration techniques to generate diverse circuit profiles, enabling comprehensive training data sets for machine learning models, demonstrating expertise in hardware/software co-design and optimization.
- Utilized TensorFlow to develop and optimize machine learning models for hardware Trojan detection, significantly reducing reconstruction errors and enhancing detection accuracy.
- Generated over 800 unique bitstreams from the FPGAs, allowing for thorough analysis of the effects of hardware trojans on circuit performance, showcasing proficiency in FPGA development tools and methodologies.
- Successfully inserted hardware trojans into ISCAS-85 circuits using Vivado software, demonstrating hands-on experience with industry-standard FPGA design tools and methodologies.
- Automated Bitstream analysis and hardware validation scripts using Python to accelerate debugging.
- Collaborated with a team of researchers to identify and document key findings regarding the insertion and detection techniques of hardware trojans, highlighting strong teamwork and communication skills.

WORK EXPERIENCE

Student Research Mentor, Project RAISE **Jun. 2024 – Aug. 2024**

- Mentored two sophomore undergraduate community college students on hardware security and machine learning, leading to two conference-ready poster presentations by the end of the program.
- Took ownership of developing a curriculum, ensuring students gained hands-on experience in Python, machine learning frameworks, and FPGA-based security testing.
- Facilitated project-based learning, contributing to a collaborative and inclusive research culture aligned with CSUF's mission.
- Participated in a panel discussion alongside two other mentors, addressing an audience of 100 students about research experiences and the supportive research environment at CSUF.

Full Stack Developer, Keka Technologies Ltd. **Jan. 2022 – Nov. 2022**

- Led the development of key features for mission-critical web applications, using cutting-edge technologies like .Net, React, Angular, Node.js, and Python. These solutions elevated application performance by 10%, ensuring optimal user engagement
- Displayed exceptional teamwork and communication skills, fostering a harmonious and productive environment among cross-functional teams. This synergy led to the on-time delivery of high-quality web applications that delighted stakeholders
- Pioneered the implementation of Continuous Integration and Continuous Deployment (CI/CD) methodologies, revolutionizing the development lifecycle. This transformative process resulted in an impressive 20% acceleration in deployment speed and streamlined workflows, acted as the primary point of contact for troubleshooting and optimizing multi-tiered systems.

Intern, Mobile Application Developer, CBIT Open-Source Community **Apr. 2021 – Jul. 2021**

- Employed Java, Kotlin, Swift, and React Native to create user-friendly mobile applications such as "News For CBIT", ensuring seamless cross-platform experiences with sustainability in mind. Designed and deployed containerized mobile applications using Docker and AWS, ensuring consistent performance across environments
- Worked collaboratively to deliver intuitive and user-centric mobile apps, promoting positive user experiences and customer satisfaction.
- Successfully implemented version control, resulting in 15% faster app deployment and efficient management of code changes, highlighting proficiency in software versioning and configuration management relevant to AI software development.

PROJECTS

FPGA Performance and Reliability Validation using an LSTM model

- Developed an ML-based framework to predict FPGA hardware failures by analyzing real-time telemetry data, including voltage fluctuations, thermal variations, and timing inconsistencies.
- Implemented anomaly detection using an LSTM-based recurrent neural network (RNN) in TensorFlow to identify deviations in dynamic power consumption and critical path delays.
- Designed a custom hardware testbench on a Xilinx Zynq-7000 FPGA, logging sensor data at a 1 kHz sampling rate to train predictive models.
- Achieved 90% precision in detecting early-stage hardware faults, reducing failure rates by 25% through proactive maintenance recommendations.

High-Speed Image Processing System Using Parallel Computing

- Utilized CUDA to parallelize computationally intensive tasks such as edge detection and feature extraction, achieving a 5x speedup compared to CPU-based systems.
- Offloaded preprocessing tasks like filtering and resizing to an FPGA, reducing overall latency by 40% and improving throughput to process 50 frames per second for 4K resolution images.
- Integrated Oracle SQL Server for relational database management, structuring tables for products, categories, users, and transactions. Conducted system optimization to minimize resource usage, achieving 90% utilization of FPGA logic elements while maintaining low power consumption of 10 W.
- Evaluated system performance using benchmark datasets like MS COCO, achieving an F1 score of 0.92 for edge detection accuracy and a processing delay of under 20 ms per frame.

GPU Workload and Perfromance Analysis

- Designed and implemented a high-performance matrix multiplication algorithm using CUDA, achieving a 5.6x speedup compared to CPU- based execution on a dataset of 10,000 x 10,000 matrices.
- Designed Utilized NVIDIA Nsight Compute to profile and optimize GPU workloads, reducing kernel execution time by 35% through memory coalescing, shared memory usage, and thread divergence minimization.
- Enabled Improved GPU resource utilization, increasing occupancy to 90% and enhancing memory bandwidth utilization by 50%. Achieved a performance comparison of 400 ms (CPU) vs. 71 ms (GPU), demonstrating near-linear scalability for larger datasets.

EDUCATION

California State University Fullerton, *Master of Science in Computer Engineering* *CGPA: **3.94**/4* **Dec. 2024**

Chaitanya Bharathi Institute of Technology, *Bachelor of Engineering in Computer Science and Engineering* **Jul. 2022**